UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/925,314	08/10/2001	Christopher R. Risucci	1778.0180000	4782

26111 7590 11/17/2004		EXAMINER
STERNE, KESSLER, GOLDSTEIN & FOX PLLC		TSAI, HENRY
1100 NEW YORK AVENUE, N.W.	ART UNIT	PAPER NUMBER
WASHINGTON, DC 20005	2183	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>9/7/04</u> .

2a)☒ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
    closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-16 and 18-20</u> is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) ___ is/are allowed.

6)☒ Claim(s) <u>1,3,8,10,15 and 18-20</u> is/are rejected.

7)☒ Claim(s) <u>2,4-7,9,11-14 and 16</u> is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____ .

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
            application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>9/7/04</u> .

4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1.   Claims 3, 10, 18, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 3, 10, and 18, it is not clear how an address can be transformed into an instruction since an address and an instruction represent different information. Some steps or details are missing.

In claim 19, it is not clear how an instruction can be transformed into an address since an address and an instruction represent different information. Some steps or details are missing.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs

of 35 U.S.C. 102 that form the basis for the rejections

under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published
> under section 122(b), by another filed in the United States before the
> invention by the applicant for patent or (2) a patent granted on an
> application for patent by another filed in the United States before the
> invention by the applicant for patent, except that an international
> application filed under the treaty defined in section 351(a) shall have the
> effects for purposes of this subsection of an application filed in the
> United States only if the international application designated the United
> States and was published under Article 21(2) of such treaty in the English
> language.

3.   Claims 1, 3, 8, 10, 15, and 18-20 are rejected under 35

U.S.C. 102(e) as being anticipated by Revilla et al. (U.S.

Patent Application Publication No. 2002/0144041), herein

referred to as Revilla et al.'041.

Referring to claims 1, 8, and 15, Revilla et al.'041

discloses as claimed a method for generating at least one

instruction for execution by a central processing unit

(execution unit 4, see Fig. 2), the method comprising the steps

of: receiving a misaligned instruction address (see page 1,

paragraph 0014, lines 5-8, regarding "the control unit 5 may

detect if an instruction is improperly aligned in memory". Note

the misaligned address is read from the (program counter in the

as Revilla et al.'041's system); causing an exception in

response to said misaligned instruction address (see page 2,

paragraph 0024, lines 1-4, regarding the control unit 5 may

generate the exception status information due to such as

misaligned addresses); and executing, in response to said

exception, an exception handling routine (inherently existing in

such as the exception handling logic 9 of the Revilla et

al.'041's system), said routine transforming data (see page 1,

paragraph 0012, lines 1-6, regarding the exception handling

logic 9 processing (transforming) the exception status

information (data) on parallel with execution of the instruction

in the execution unit 4) into at least one instruction (the

instruction is best broadly and reasonably interpreted as the

instruction passing from exception handling logic 9 to

instruction alignment unit 8 in Fig. 1, or the micro instruction

passing to execution unit 4 internally) for execution by the

central processing unit (execution unit 4, see Fig. 2).

Referring to claim 20, Revilla et al.'041 discloses as

claimed, as best understood, a computer system (comprising 2,

see Fig. 1), comprising: a processor (2, see Fig. 1); a memory

(inherently existing in the Revilla et al.'041's system see Fig.

1), coupled to said processor; and sequences of instructions

(inherently existing in the memory of the Revilla et al.'041's

system see Figs. 1 and 4) stored in said memory which when

executed by said processor cause said processor to: receive a

misaligned instruction address (see page 1, paragraph 0014,

lines 5-8, regarding "the control unit 5 may detect if an

instruction is improperly aligned in memory". Note the

misaligned address is read from the (program counter in the as

Revilla et al.'041's system); execute an exception in response

to said misaligned instruction address (see page 2, paragraph

0024, lines 1-4, regarding the control unit 5 may generate the

exception status information due to such as misaligned

addresses); and transform data stored in said memory (see page

1, paragraph 0012, lines 1-6, regarding the exception handling

logic 9 processing (transforming) the exception status

information (data, from memory, see Fig. 4) on parallel with

execution of the instruction in the execution unit 4) into valid

processor instructions (the instruction is best broadly and

reasonably interpreted as the instruction passing from exception

handling logic 9 to instruction alignment unit 8 in Fig. 1, or

the micro instruction passing to execution unit 4 internally) in

response to said exception.

As to claims 3, and 10, Revilla et al.'041 also discloses,

as best understood, transforming said misaligned instruction

address (the instruction to cause the exception due to

misaligned address, see also page 1, paragraph 0014, lines 5-8,

regarding "the control unit 5 may detect if an instruction is

improperly aligned in memory") into said at least one ins (the

instruction is best broadly and reasonably interpreted as the

instruction passing from exception handling logic 9 to

instruction alignment unit 8 in Fig. 1, or the micro instruction

passing to execution unit 4 internally).

As to claim 18, Revilla et al.'041 also discloses, as best

understood, means for transforming said misaligned instruction

address (the instruction to cause the exception due to

misaligned address, see also page 1, paragraph 0014, lines 5-8,

regarding "the control unit 5 may detect if an instruction is

improperly aligned in memory") into said at least one ins (the

instruction is best broadly and reasonably interpreted as the

instruction passing from exception handling logic 9 to

instruction alignment unit 8 in Fig. 1, or the micro instruction

passing to execution unit 4 internally).

As to claim 19, Revilla et al.'041 also discloses, as best

understood, means for transforming said misaligned instruction

(the instruction to cause the exception due to misaligned

address, see also page 1, paragraph 0014, lines 5-8, regarding

"the control unit 5 may detect if an instruction is improperly

aligned in memory") into a memory address and for using said

memory address to fetch said at least one instruction (<u>the
instruction is best broadly and reasonably interpreted as the
instruction passing from exception handling logic 9 to
instruction alignment unit 8 in Fig. 1, or the micro instruction
passing to execution unit 4 internally</u>) from memory.

Allowable Subject Matter

4.   Claims 2, 4-7, 9, 11-14, and 16 are objected to as being
dependent upon a rejected base claim, but would be allowable if
rewritten in independent form including all of the limitations
of the base claim and any intervening claims.

Response to Amendment

5.   Applicant's arguments filed 9/3/04 have been fully

considered but they are not deemed to be persuasive.

Regarding 35 U.S.C. 112, second paragraph rejections to

claims 3, 10, 18, and 19, Applicants described the detailed data

transformation in the specification. However, the claim

language in the claims is still not understandable and

indefinite.

Applicants argue that "The present invention operates by

"transforming data into at least one instruction" that can be

executed by a processor. This claimed feature of the present

invention, recited in amended independent claim 1, 8, and 15, is

neither disclosed or suggested by Revilla"; and "Revilla does

not disclose or suggest at least the "transformation data"

feature of the present invention recited in claim 20 ".

Examiner disagrees with Applicants. As set forth in the art

rejections, Revilla et al.'041 discloses: transforming data (see

page 1, paragraph 0012, lines 1-6, regarding the exception

handling logic 9 processing (transforming) the exception status

information (data) on parallel with execution of the instruction

in the execution unit 4) into at least one instruction (the

instruction is best broadly and reasonably interpreted as the

instruction passing from exception handling logic 9 to
instruction alignment unit 8 in Fig. 1, or the micro instruction
passing to execution unit 4 internally).

Conclusion

6.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the
extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action
is set to expire THREE MONTHS from the mailing date of this
action. In the event a first reply is filed within TWO MONTHS
of the mailing date of this final action and the advisory action
is not mailed until after the end of the THREE-MONTH shortened
statutory period, then the shortened statutory period will
expire on the date the advisory action is mailed, and any
extension fee pursuant to 37 CFR 1.136(a) will be calculated
from the mailing date of the advisory action. In no event,
however, will the statutory period for reply expire later than
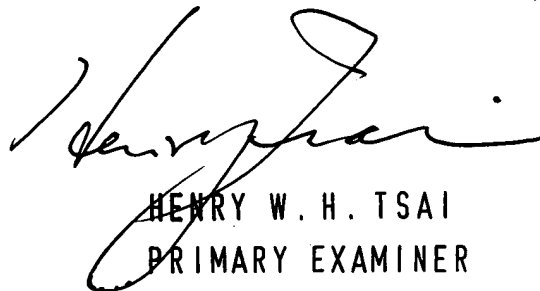SIX MONTHS from the mailing date of this final action.

Contact Information

7.   Any inquiry concerning this communication or earlier
communications from the examiner should be directed to Dr. Henry

Tsai whose telephone number is (571) 272-4176. The examiner can

normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful,

the examiner supervisor, Eddie Chan, can be reached on (571)

272-4162. Any inquiry of a general nature or relating to the

status of this application or proceeding should be directed to

the TC central telephone number, (571) 272-2100.

8.   In order to reduce pendency and avoid potential delays,

Group 2100 is encouraging FAXing of responses to Office actions

directly **into the Group at fax number: 703-872-9306.** This

practice may be used for filing papers not requiring a fee. It

may also be used for filing papers which require a fee by

applicants who authorize charges to a PTO deposit account.

Please identify the examiner and art unit at the top of your

cover sheet. Papers submitted via FAX into Group 2100 will be

promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
November 15, 2004